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SiC epitaxial surface defect characterization

This application notes introduces a nondestructive method to characterize the growth-pit surface defects and their possible influence on SiC device performances. Compared to the crystallographic defects in SiC, the existence of sharp-apex small growth pits was revealed only a few years ago [reference 1-4]. Growth pits have not been captured in the past because they are submicron in size and usually associated with crystallographic defects. They are barely detectable under Nomarski optical microscope and could be easily neglected under AFM investigation since their density is relatively low (about $10^3/cm^2$) compared to the high magnification of AFM.

In order to improve the SiC device performance and fabrication yield, the correlation between device performance and defects has been extensively investigated in the past decade. However, a clear correlation between defects and device issues, such as Schottky barrier height (SBH) inhomogeneities in SiC Schottky diodes, could not be established. Due to the lack of effective characterization tools, the investigated surface-morphologic defects influence on device performance were limited to those with a relatively large size, which are usually visible under a normal optical microscope. There were few efforts that have been dedicated to investigate the influence of these sharp-apex growth pits on SiC device.

In order to detect the growth pits associated with different crystallographic defects, areas with screw dislocations, stressed striations, and grain boundaries (or dislocation walls) were identified and imaged by PLM. An atomic force microscope (AFM) was then used to scan the corresponding areas selected by PLM to identify the surface morphological defects. After the specific growth pits were located, a higher magnification AFM scan was used to further reveal the detailed structures of the growth pits. PLM is the defect delineation technique which nondestructively maps micropipes, screw dislocations, grain boundaries and stressed zones in SiC on a wafer-scale. One unique feature of the PLM system is its ability to characterize a SiC wafer with an epilayer, providing a newly found opportunity to nondestructively correlate the different growth pits on a SiC epi-surface corresponding to different crystallographic defects and to determine the source of small growth pits.

Using PLM and AFM, various growth pits associated with crystallographic defects in 4H silicon carbide (SiC) epilayer can be extensively investigated. Defects including screw dislocations, grain boundaries and edge dislocations open growth pits of various shapes in SiC epilayer surface (Figures 1-4). In 10 µm thick epilayers, the previously reported small triangular growth pits can be further classified into growth pits with or without nano-cores (Figure 4). The growth pits with nano-cores are associated with screw dislocations while the growth pits without nano-cores are mainly observed in the highly stressed regions of the crystal (Figure 3). The grain boundaries result in growth-pit arrays (Figure 2), while the edge dislocations lead to shallow stripe-shaped growth pits in 10 µm

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thick epilayers (Figure 1) and growth pits with small nano-cores in 100 μm thick epilayers.

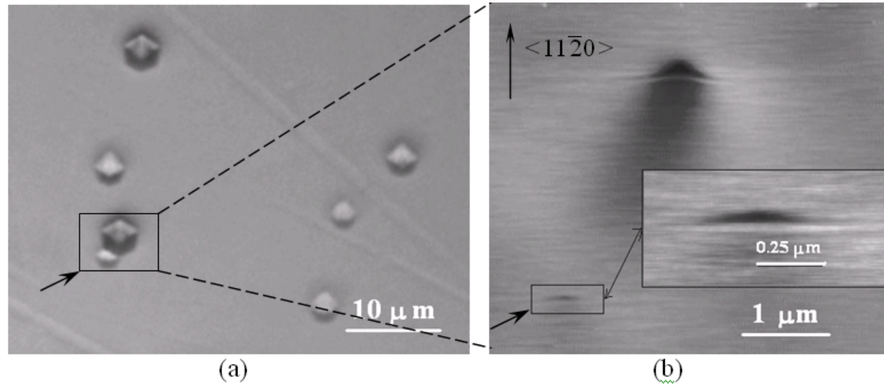

Figure 1, individual growth pits associated with edge and edge dislocations (a) molten KOH etching pits (optical), (b) the corresponding growth pit (AFM)

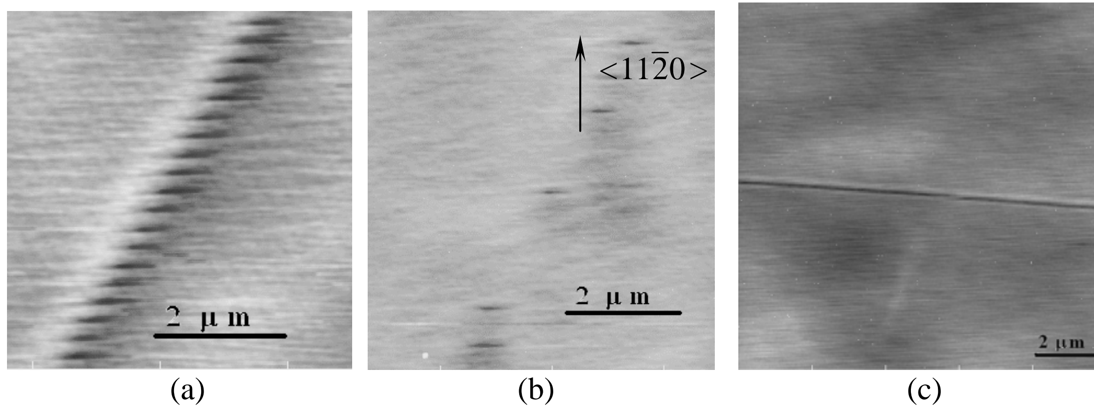

Figure 2, AFM images of growth pits associated with (a) a PLM stress striation pattern, (b) a PLM dislocation-wall pattern, and (c) a PLM stress striation pattern perpendicular to the $<11\bar{2}0>$ direction

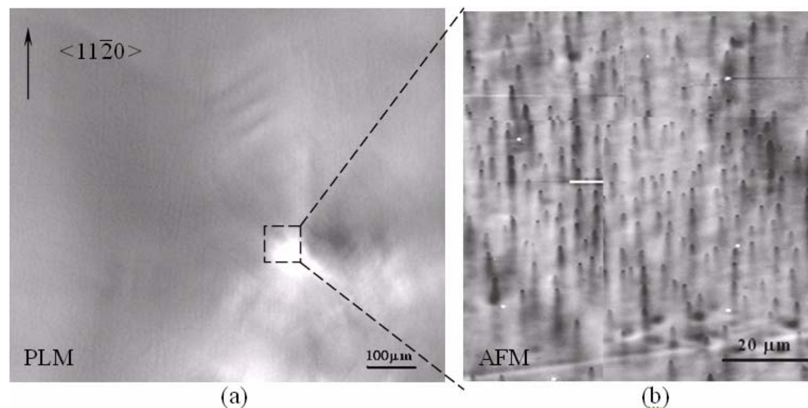

Figure 3, High density of growth pits found in a highly stress area (10 μm epilayer): (a) a highly stressed zone identified by PLM (b) corresponding growth pits (AFM)

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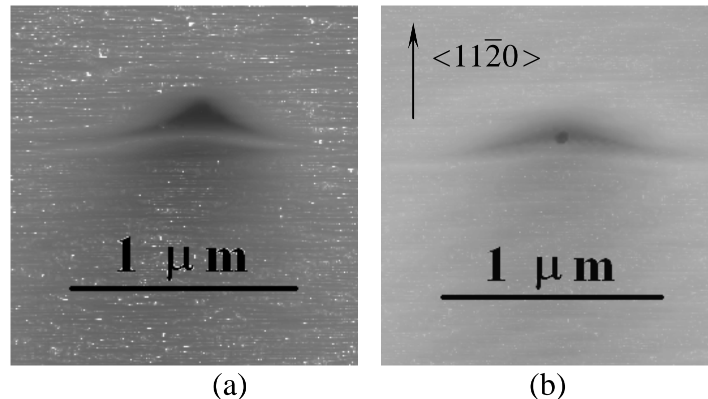

(a) (b)

Figure 4, AFM images of growth pits associated with PLM screw-dislocation patterns in 10 μm epilayers: (a) growth pit with out nano-core, (b) growth pit with nano-core

Though growth pits might disappear as the SiC epi-growth technology improves in the future, currently the growth pit influence on SiC device performance has been neglected. Sharp-tipped and nano-core structure of these small growth pits could inevitably cause the junction distortion and electric field enhancement in both Schottky and pn junctions, and degrade the corresponding device performance. The sharp apex growth pits and nano-cores occur and their sizes increase as the thickness of epilayer increases, it is expected that the growth pits influence on device performance would also increase. It might be more complicated in the case of a thick epilayer (> 50 μm) used for high-voltage SiC devices, since the small growth pits with nano-cores, associated with edge dislocations, would occur in these SiC epilayers.

For more information about growth pits investigation, please check reference 4. For results about device and growth pits correlation, please check the application note entitled "Schottky barrier inhomogeneities in SiC Schottky contacts".

Reference:

[1] "Correlation of EBIC and SWBXT imaged defects and epilayer growth pits in 6H-SiC Schottky diodes," *Material Science Forum*, Vol. 338-342, 2000: 489.
[2] "Investigations of non-micropipe X-ray imaged crystal defects in SiC devices," *Material Research Society Symposia Proceed*ings, Vol. 622, 2000: T1.2.
[3] "Nondestructive defect characterization of SiC substrates and epilayers," *Journal of Electronic Material*, Vol. 33, 2004: 450-455.
[4] "Investigation on Small Growth Pits in 4H Silicon Carbide Epilayers," *Journal of Crystal Growth*, Vol. 279, 2005: 425-432.

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